11/14/00

A

JC915 U.S. PTO 11/13/00

PTO/SB/05 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office U S. DEPARTMENT OF COMMERCE

Please type a plus sign (+) inside this box → +

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**TI-20390**
First Inventor	**Sami Kiriaki**
Title	**ANALOG MULTIPLEXERS WITH CMOS CONTROL SIGNALS**
Express Mail Label No.	**EL552916238US**

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

JC688 U.S. PTO 09/711714 11/13/00

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original, and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 22] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 6]
5. Oath or Declaration [*Total Pages*]
   - a. [X] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1 63(d)) *(for continuation/divisional with Box 18 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1 33(b)
6. [ ] Application Data Sheet. See 37 CFR 1 76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Form (CRF)
   - b. Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies); or
     - ii. [ ] paper
   - c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & documents(s))
10. [ ] 37 CFR 3 73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [X] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent
17. [ ] Other.

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____

Prior application information Examiner _____ *Group / Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* **23494** *(Insert Customer No or Attach bar code label here)* or [X] *Correspondence address below*

NAME	**Texas Instruments Incorporated**				
ADDRESS	**Mark E. Courtney**				
	P.O. Box 655474, MS 3999				
CITY	**Dallas**	*STATE*	**TX**	*ZIP CODE*	**75265**
COUNTRY	**USA**	*TELEPHONE*	**(972) 917-5632**	*FAX*	**(972) 917-4418**

Name (Print/Type)	**Carlton H. Hoel**	*Registration No. (Attorney/Agent)*	**Reg. No. 29,934**
Signature		*Date*	**11/13/00**

Burden Hour Statement: This form is estimated to take 0 2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective November 10, 1998
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT ($) 710

Complete If Known	
Application Number	
Filing Date	11/13/00
First Named Inventor	Sami Kiriaki
Examiner Name	TBD
Group / Art Unit	TBD
Attorney Docket No.	TI-20390

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

☒ Charge any additional fee required or credit any overpayment

☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	710	201	380	Utility filing fee	710
106	310	206	155	Design filing fee	$
107	480	207	240	Plant filing fee	$
108	760	208	380	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$

SUBTOTAL (1) ($)710

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims 10	-20**= 0	x	18	=	0
Independent Claims 3	-3** = 0	x	78	=	0
Multiple Dependent			260	=	0

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent Claims in excess of 3
104	260	204	130	Multiple dependent claims in excess of 3
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension of time within second month	
117	870	217	435	Extension of time within third month	
118	1,360	218	680	Extension of time within fourth month	
128	1,850	228	925	Extension of time within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per properly (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1 129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Carlton H. Hoel	Reg Number	29,934
Signature		Date 11/13/00	Deposit Account User ID

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

	Sami Kiriaki	Docket No.:	TI-20390
Serial No.:	TBD	Examiner:	TBD
Filed:	11/13/00	Art Unit:	TBD

For: **ANALOG MULTIPLEXERS WITH CMOS CONTROL SIGNALS**

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner

of Patents

Washington, D.C. 20231

"EXPRESS MAILING" Mailing Label No. **EL552916238US**

Date of Deposit: November 13, 2000.

Please amend the above referenced Application as follows:

In the Specification:

Page 1, before line 1, insert --This application claims priority under 35 USC §119(e)(1) of provisional application number 60/164,996 filed 11/12/99.--

REMARKS

Entry of the foregoing amendment prior to examinations is respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Carlton H. Hoel
Attorney for Applicant
Reg. No. 29,934

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5632

ANALOG MULTIPLEXERS WITH CMOS CONTROL SIGNALS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to fast analog multiplexers with CMOS control signals and particularly to the elimination of cross-signal feed-through in these high speed circuits.

2. Brief Description of the Known Art

Figure 1a shows the simplest type of conventional analog multiplexer 1 (MUX) built with CMOS switches. Here, the MUX switches are comprised of n-channel MOS transistors 2-4 and p-channel MOS transistors 5-7, connected in parallel to form a CMOS switch. This shows a n-to-1 MUX with input signals sig $_1$, sig $_2$, ... sig $_n$ connected to MUX switches 2/5, 3/6, and 4/7, respectively. The output of the MUX switches are connected together and become the output of the MUX circuit. The MUX switches are controlled by placing complementary control voltages on the transistor gates, as shown. The logic circuit for generating these control signals is comprised of two inverters 8 and 9, as shown in Figure 1b. As example, for operation between 0 volts and positive power supply V_{DD},

the switches are turned "ON" and "OFF" at their gates, as follows:

	n-Channel Transistor	p-Channel Transistor
ON	V_{DD}	0V
OFF	0V	V_{DD}

where V_{DD} is the positive power supply (e.g. +5V) and 0V is ground.

By having the n-channel and p-channel transistors connected in parallel, the circuit can handle signals from 0 to V_{DD} volts, as illustrated in Figure 1c. In this figure, V_{sig} is plotted on the abscissa and the ON resistance of the switches, R_{SW}, is plotted on the ordinate. The transistors tend to be "ON" over the following voltage ranges, respectively:

$$\text{n-channel:} \quad 0 \rightarrow [V_{DD} - V_{th(n\text{-}ch)}]$$

$$\text{p-channel} \quad V_{DD} \rightarrow [0 + V_{th(p\text{-}ch)}]$$

This means that for small signals the n-channel transistor is primarily used and for large signals the p-channel transistor is primarily used. Also, the ON resistance, R_{SW}, tends to be optimal (lowest) in mid-signal range where both parallel transistors are ON.

The primary problem with analog multiplexers of this type, used to select one of several input signals, is that they often have undesirable signal feed-through where an attenuated level of an unselected signal appears as part of the output signal. This feed-through is due primarily to the parasitic capacitances, C_{gd} and C_{gs}, associated with the CMOS transistors used to implement the switches. As a result, this undesirable feed-through causes a degradation at the output of both the signal-to-noise ratio (SNR) and the signal-to-distortion ratio (SDR) for the selected signal at the output of the MUX.

Thus, there is a need for an improved high speed MUX which eliminates the cross-signal feed-through problems of the prior art. The invention and embodiment disclosed herein address this need.

For reference, U. S. Patents 5,744,995 discusses multi-input multiplexers and U. S. patent 5,598,114 discusses high-speed multiplexers.

SUMMARY OF THE INVENTION

This invention addresses the shortcomings of prior art analog multiplexers, depending on the application, to provide low-distortion, high-speed solutions. The objective is to provide high-speed multiplexers which eliminates cross-signal feed-through at the circuit's output. These designs take into account such parameters as input signal level, signal bandwidth, common mode operation, parasitic capacitance, and transistor layout.

The circuits of this invention use N-MOS/P-MOS transistor pairs for signal switches and additional N_MOS transistors to effectively shunt the unselected signal paths to circuit ground, thereby considerably reducing the amount of undesired signal presence at the circuit's output.

Two embodiments of the invention address the signal feed-through issue with CMOS circuitry; one for limited bandwidth applications and one for small signal applications. For small signal applications, the P-MOS transistors in the signal switches of these circuits are eliminated, leaving only the N-MOS transistors, to provide improved bandwidth and lower signal feed-through. All of the techniques of this invention can be applied to both single-ended and/or differential configurations.

Also, the layout of CMOS transistors with reduced parasitic capacitance, used in the implementation of the circuits of this invention, are included in the discussion.

5

BRIEF DISCRIPTION OF THE DRAWINGS

The included drawings are as follows:

Figure 1a shows a schematic for a simple analog MUX with CMOS control. (prior art)

Figure 1b shows a typical schematic of the control logic for an analog MUX. (prior art)

Figure 1c illustrates the switching characteristics for the n-channel and p-channel transistors commonly used in the analog MUX circuitry. (prior art)

Figure 2 shows the schematic for a CMOS MUX of this invention with improved input signal feed-through.

Figure 3 shows the schematic for a small-signal, high-bandwidth, single-ended CMOS MUX of this invention with improved input signal feed-through.

Figure 4 shows the schematic for a small-signal, high-bandwidth, differential CMOS MUX of this invention with improved input signal feed-through.

Figures 5a and 5b illustrate the layout of the CMOS transistors of this invention with reduced parasitic output capacitance for use in analog multiplexer applications.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 shows one embodiment for a CMOS MUX 10 with improved signal feed-through characteristics. The circuit is comprised of an input pair of n-channel 11-13/p-channel 17-19 MOS transistor switches and an output pair of n-channel 14-16/p-channel 20-22 MOS transistor switches connected in series at each input and additional n-channel MOS transistors 23-25 connected, as pull-down devices, between each series transistor pair and circuit ground. Input signals Sig_1, Sig_2, and Sig_n are connected to transistors pairs 11/17, 12/18, and 13/19, respectively. The outputs of MOS transistor pairs 14/20, 15/21, and 16/22 are tied together to form a low feed-through output signal. Each of the series n-channel MOS transistors 11-16 are driven at the gate by logic control signals, S_n, while the series p-channel MOS transistors 17-22 and n-channel MOS pull-down transistors 23-25 are driven by logic control signals, $\overline{S_n}$, which are complementary to the above 11-16. As a result, the overall effect of this circuit arrangement is as though there were individual switches, with low signal feed-through, for each input signal.

In operation, when one signal is selected, all other signals are shunted to ground by their associated pull-

down transistors, such that feed-through from the unselected signals is eliminated at the output. For example, if Sig $_2$ is selected, then MOS pull-down transistor switch 24 is OFF, allowing the Sig $_2$ signal to pass through to the output while MOS pull-down transistors 23 and 25 are ON, shunting any feed-through from signals Sig $_1$ and Sig $_n$ to ground and preventing any feed-through of these unselected signals at the output. Either the n-channel or p-channel MOS transistor can be selected as the ON switch, depending on the level of the input signal.

This circuit is limited to rather low bandwidth applications due to the total RC time constant associated with each switch. For example, switch SW1x 11/17 has an ON resistance of R_{1X} and a total parasitic capacitance C_{1X} at node N_1 and switch SW1y 14/20 has an ON resistance of R_{1Y} and a total parasitic capacitance C_{1Y} at the output node. Therefore, the total RC time constant for Sig $_1$ is given as:

$$R_{1X} \cdot C_{1X} + R_{1Y} \cdot C_{1Y}$$

For a given switch control level and common mode signal, the switch ON resistance can be reduced by increasing the widths of both the N-MOS and P-MOS transistors. However,

this reduction in ON resistance is typically accompanied by an increase in the drain-to-bulk and source-to-bulk parasitic capacitance. But, an optimum design can be found for a limited number of signals that are joined together at the MUX output for a given application.

In a second embodiment of the circuit 26, for the case of small signal applications where the input signal is a small fraction of the MUX supply voltage, the switch bandwidth can be improved by modifying the circuit as shown in Figure 3. Since the mobility of electrons is approximately three times greater than that for holes, the problem with the ON switch resistance discussed above is magnified by the fact that P-MOS device sizes must be made three times or more the size of the N-MOS devices to overcome this mobility difference. However, this larger size for the P-MOS devices results in larger parasitic capacitance which in turn increases the RC time constant and reduces the switch bandwidth. In this circuit, used primarily for small signal applications, the p-channel MOS transistors 17-22 (in Figure 2) are eliminated completely so that the series switches consists of only n-channel MOS transistor switches 11-16 and the n-channel MOS shunting transistors 23-25. Otherwise, the circuit configuration is the same as in Figure 2. In this circuit the parasitic capacitance is reduced by as much

as 50%, assuming the signal common mode level is closer to the MUX ground and the peak-to-peak signal level is a small fraction of the MUX supply voltage. This configuration is applicable as long as the signal voltage level (V_{cm}+ V_{sig}) produces enough V_{gs} for the series N-MOS transistors 11-16 to maintain a low ON resistance.

The circuits discussed above are shown for single-ended signal applications. However, all these circuits can be implemented for fully differential operation, as illustrated in Figure 4 for the small signal circuit discussed above. This circuit is essentially comprised of two of the single-ended circuits 26 coupled so as to provide for differential inputs signals Sig_1+/Sig_1-, Sig_2+/Sig_2-, Sig_n+/Sig_n- and a differential output signal Sig_O+/Sig_O-.

The parasitic capacitance in these high-speed MUX circuits can be further reduced by using an even number of "fingers" in the circuit layout of the series output transistors SW1y 14, SW2y 15, SWny 16, as illustrated in Figures 5a and 5b. Figure 5a shows a typical layout for a single finger N-MOS transistor which is comprised of a source 27, a gate 28, and a drain 29. In this case the source and drain capacitances are equal and given as the

area of the gate width (w) and drain/source length (x), as follows:

$$C_S = C_D = x \cdot w$$

On the other hand, for the lower capacitance layout of this invention, shown in Figure 5b, the gate and source are split into two parts, or "fingers", so that the transistor is comprised of sources 30 and 31, gates 32 and 33, and drain 34, and the capacitance-to-area relationship becomes:

$$C_D = x \cdot \frac{w}{2}, \quad \text{and}$$

$$C_S = 2 \cdot x \cdot \frac{w}{2} = x \cdot w, \text{ so that}$$

$$C_S = 2 \cdot C_D .$$

This means that a two "finger" device has a drain-to-bulk parasitic capacitance, C_{dB}, that is one-half the source capacitance, C_S, and as a result the total output capacitance is reduced by at least 50%. This layout can be used to obtain a significant boost, where the bandwidth of the MUX circuit is at least doubled.

While the invention has been described in the context of two preferred embodiments, it will appear to those skilled in the art that the present invention may be

modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

I CLAIM:

1. A CMOS analog multiplexer circuit comprising:

multiple series n-channel/p-channel MOS transistor input switches;

multiple series n-channel/p-channel MOS transistor output switches;

multiple pull-down n-channel MOS transistor switches; wherein

said circuit prevents cross-signal feed-through from unselected inputs by shunting said feed-through to circuit ground.

2. The CMOS analog multiplexer circuit of Claim 1 further comprising:

the input of a first series input n-channel/p-channel MOS transistor switch coupled to the first circuit input signal;

the input of a second series input n-channel/p-channel MOS transistor switch coupled to the second circuit input signal;

the input of a nth series input n-channel/p-channel MOS transistor switch coupled to the nth circuit input signal;

the output of said first series input n-channel/p-channel MOS transistor switch coupled to the input

of a first output n-channel/p-channel MOS transistor switch and to the drain of a first n-channel MOS pull-down transistor;

the output of said second series input n-channel/p-channel MOS transistor switch coupled to the input of a second output n-channel/p-channel MOS transistor switch and to the drain of a second n-channel MOS pull-down transistor;

the output of said nth series input n-channel/p-channel MOS transistor switch coupled to the input of a nth output n-channel/p-channel MOS transistor switch and to the drain of a nth n-channel MOS pull-down transistor;

the outputs of said first, second, and nth output n-channel/p-channel MOS transistor switches coupled together and to circuit output;

the sources of said first, second, and nth n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said series input and output p-channel MOS transistor switches and all n-channel MOS pull-down transistors coupled to a logic control

signal which is the complement of said input/output transistor logic control signal.

3. The CMOS analog multiplexer circuit of Claim 2, further comprising MOS transistor layouts which have an even number of circuit fingers: wherein said MOS transistor's parasitic capacitance is reduced by more than 50%; and said MOS transistor's bandwidth is at least doubled.

4. The CMOS transistor layout of Claim 3 further comprising:
a CMOS transistor whose architecture has the source and gate split in half such that it consists of the sequence: one-half source, one-half gate, drain, one-half gate, and one-half source;
said CMOS transistor whose drain capacitance is half that of a conventional CMOS transistor;
said CMOS transistor whose gate is split into two parts each having a width of w/2;
said CMOS transistor whose source is split into two parts each having a width of w/2;
said two gate parts coupled together and to transistor gate output;
said two source parts coupled together and to transistor source output.

5. A CMOS analog multiplexer circuit comprising:

multiple series n-channel MOS transistor input switches;

multiple series n-channel MOS transistor output switches;

multiple n-channel MOS transistor pull-down switches; wherein

said circuit is capable of multiplexing small level analog signals having amplitudes which are a small fraction of the power source;

said circuit's parasitic capacitance is reduced by as much as 50%;

said circuit's bandwidth is at least doubled; and

said circuit prevents cross-signal feed-through from unselected inputs by shunting said feed-through to circuit ground.

6. The CMOS analog multiplexer circuit of Claim 5 further comprising:

the input of a first series input n-channel MOS transistor switch coupled to the first circuit input signal;

the input of a second series input n-channel MOS transistor switch coupled to the second circuit input signal;

the input of a nth series input n-channel MOS transistor switch coupled to the nth circuit input signal;

the output of said first series input n-channel MOS transistor switch coupled to the input of a first output n-channel transistor switch and to the drain of a first n-channel MOS pull-down transistor;

the output of said second series input n-channel MOS transistor switch coupled to the input of a second output n-channel MOS transistor switch and to the drain of a second n-channel MOS pull-down transistor;

the output of said nth series input n-channel MOS transistor switch coupled to the input of a nth output n-channel MOS transistor switch and to the drain of a nth n-channel MOS pull-down transistor;

the outputs of said first, second, and nth output n-channel MOS transistor switches coupled together and to the circuit output;

the sources of said first, second, and nth n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said n-channel MOS pull-down transistors coupled to a logic control signal which is the complement of said series input/output transistor logic control signal.

7. A CMOS analog multiplexer circuit for use with differential input signals, comprising:

multiple positive and negative signal series n-channel MOS transistor input switches;

multiple positive and negative signal series n-channel MOS transistor output switches;

multiple positive and negative signal n-channel MOS transistor pull-sown switches; wherein

said series positive and negative MOS transistor switch's capacitacne is reduced by at least 50% by means of eliminating the p-channel MOS transistors;

said circuit's bandwidth is at least doubled by means of eliminating said p-channel MOS transistors;

said circuit is capable of multiplexing small level analog signals having amplitudes which are a small fraction of the power source; and

said circuit prevents cross-signal feed-through from unselected inputs by shunting said feed-through to circuit ground.

8. The CMOS analog multiplexer circuit of Claim 7 further comprising:

the positive inputs of multiple differential input signals coupled to corresponding multiple positive input series n-channel MOS transistor switches, respectively;

the outputs of said multiple positive input series input n-channel MOS transistor switches coupled to the inputs of multiple positive output n-channel MOS transistor switches, respectively, and to the drains of multiple positive n-channel MOS pull-down transistors;

the outputs of said multiple positive output n-channel MOS transistor switches coupled together and connected to the positive differential circuit output;

the sources of said multiple positive n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said positive series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said positive n-channel MOS pull-down transistors coupled to a logic control signal that is complementary to said positive series input/output logic control signal;

the negative inputs of multiple differential input signals coupled to corresponding multiple negative input series n-channel MOS transistor switches, respectively;

the outputs of said multiple negative input series input n-channel MOS transistor switches coupled to the inputs of multiple negative output n-channel MOS transistor switches, respectively, and to the drains of multiple negative n-channel MOS pull-down transistors;

the outputs of said multiple negative output n-channel MOS transistor switches coupled together and connected to the negative differential circuit output;

the sources of said multiple negative n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said negative series input and output n-channel MOS transistor switches coupled to a logic control signal;

the gates of all said negative n-channel MOS pull-down transistors coupled to a logic control signal that is complementary to said negative series input/output logic control signal.

9. The CMOS analog multiplexer circuit of Claim 6 or 8 further comprising MOS transistor layouts having an even number of circuit fingers: wherein
said MOS transistor's parasitic capacitance is further reduced by more than 50%; and
said MOS transistor's bandwidth is further improved by at least two times.

10. The CMOS transistor layout of Claim 9 further comprising:
a CMOS transistor whose architecture has the source and gate split in half such that it consists of the sequence: one-half source, one-half gate, drain, one-half gate, and one-half source;
said CMOS transistor whose drain capacitance is half that of a conventional CMOS transistor;
said CMOS transistor whose gate is split into two parts each having a width of w/2;
said CMOS transistor whose source is split into two parts each having a width of w/2;
said two gate parts coupled together and to transistor gate output;
said two source parts coupled together and to transistor source output.

ANALOG MULTIPLEXERS WITH CMOS CONTROL SIGNALS

ABSTRACT

Analog multiplexer circuits with CMOS control signals and with low signal feed-through and high bandwidth are described. These circuits emphasize low parasitic capacitance through circuit layout techniques and the use of smaller size n-channel transistors where possible. These circuits can be used for both single-ended and differential configurations. Two embodiments of the circuit are discussed allowing for optimal selection of multiplexers in application requirements ranging from lower-to-higher bandwidth and small-to-large input signal size.

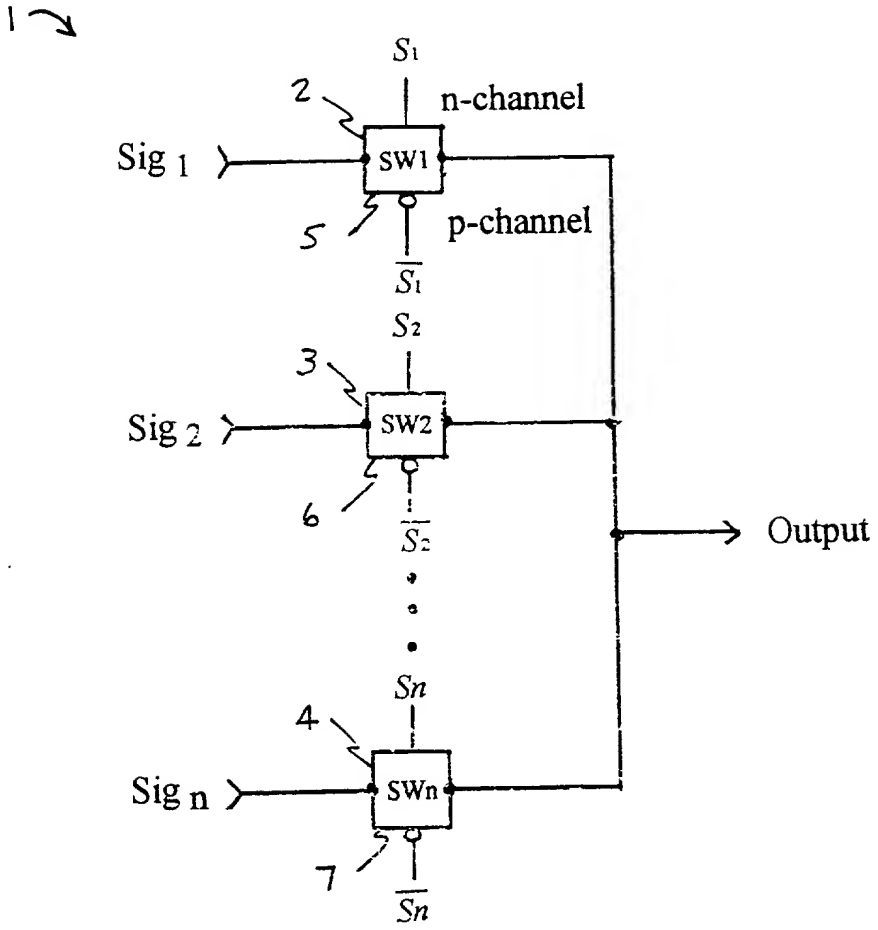

Fig. 1a

prior art

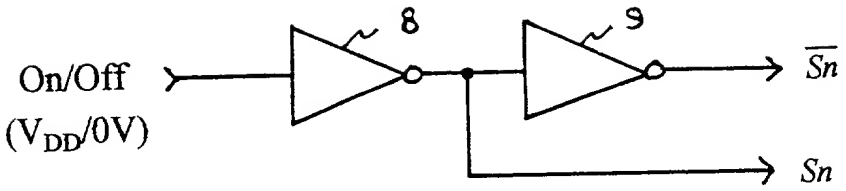

Fig. 1b

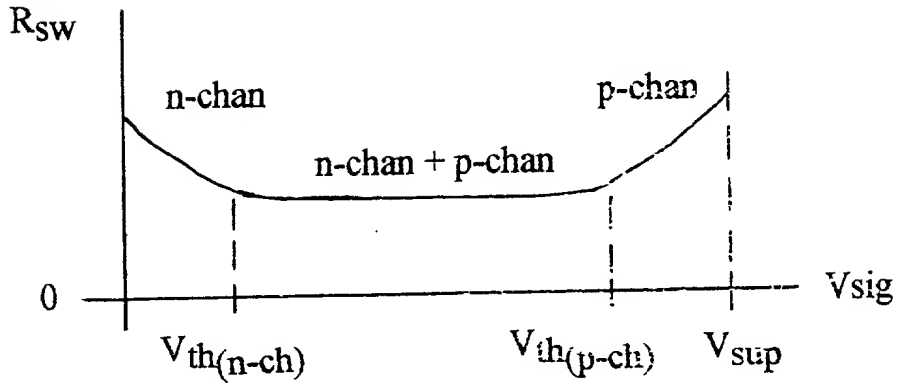

Fig. 1c

prior art

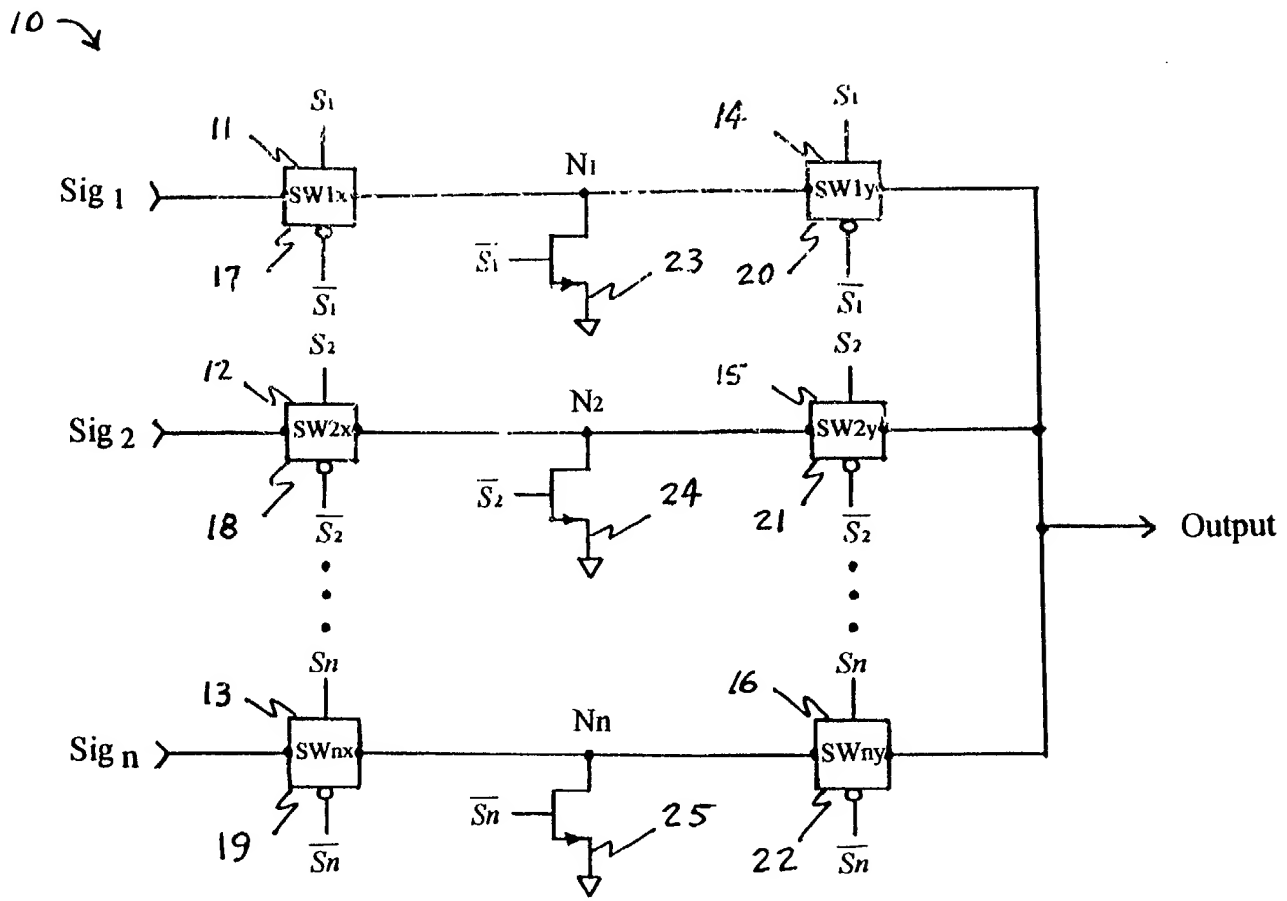
10
11
14
12
15
13
16
17
18
19
20
21
22
23
24
25
Sig 1
Sig 2
Sig n
SW1x
SW1y
SW2x
SW2y
SWnx
SWny
N1
N2
Nn
S1
S2
Sn
Output

Fig. 2

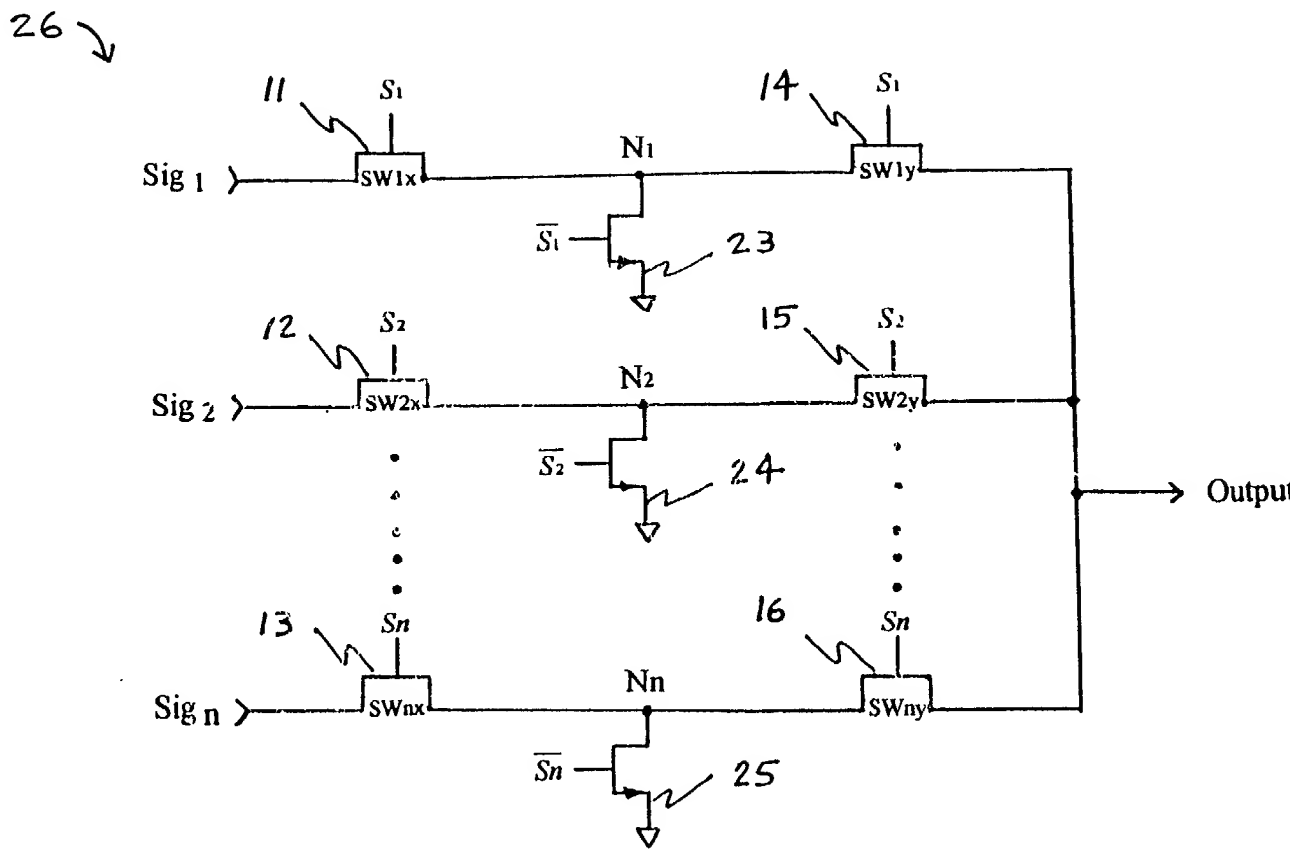
26
11
12
13
14
15
16
23
24
25
Sig 1
Sig 2
Sig n
SW1x
SW2x
SWnx
SW1y
SW2y
SWny
N1
N2
Nn
S1
S2
Sn
Output

Fig. 3

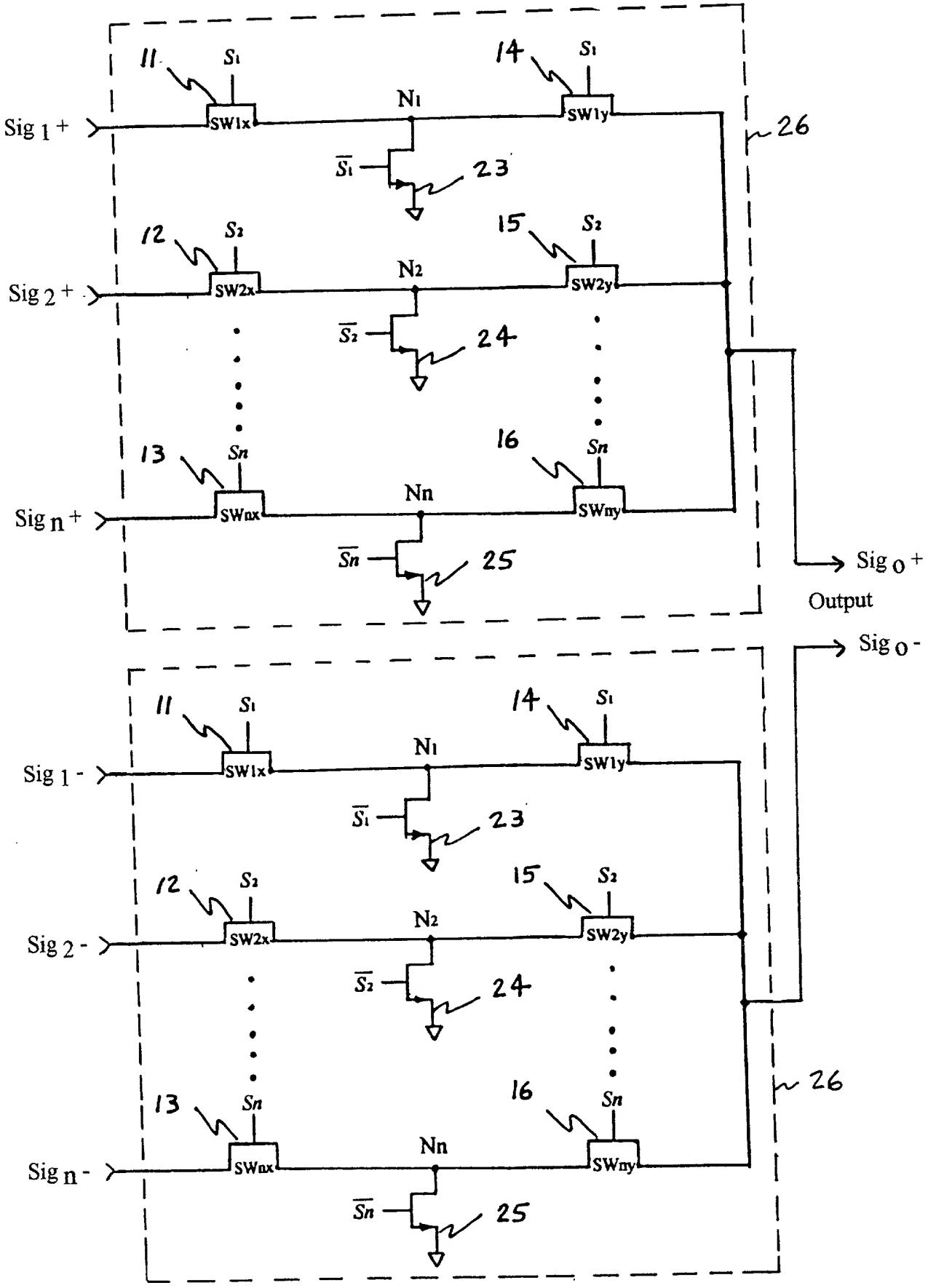
Sig 1 +
Sig 2 +
Sig n +
Sig o +
Output
Sig o -
Sig 1 -
Sig 2 -
Sig n -
11
12
13
14
15
16
S1
S2
Sn
SW1x
SW2x
SWnx
SW1y
SW2y
SWny
N1
N2
Nn
23
24
25
26

Fig. 4

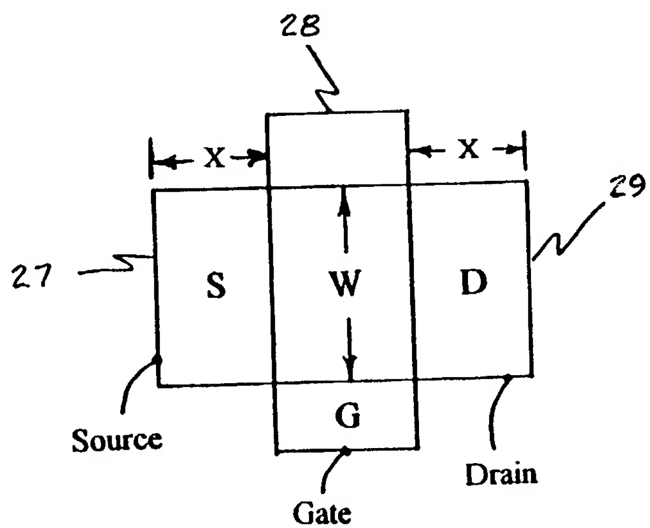
28
X
X
29
27
S
W
D
G
Source
Gate
Drain

Fig. 5a

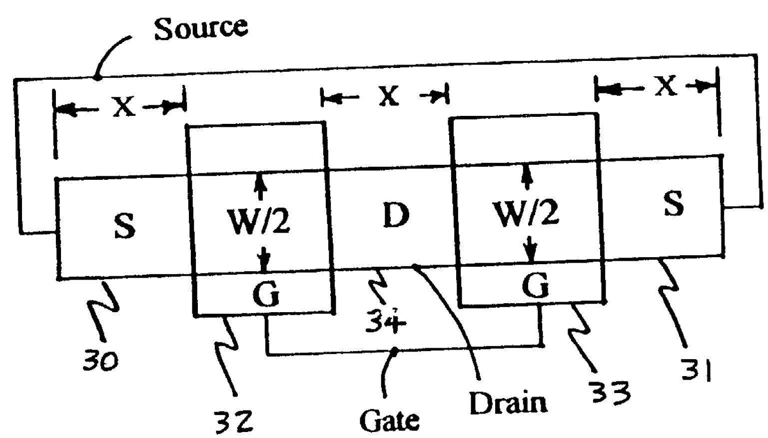
Source
X
X
X
S
W/2
D
W/2
S
G
G
30
34
32
Gate
Drain
33
31

Fig. 5b

TI Docket No
TI-20390

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: **Analog Multiplexers With CMOS Control Signals**		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH Robby T. Holland, Reg. No. 33,304; W. James Brady III, Reg. No. 32,080; Alan T. Stewart, Reg. No. 35,373; Mark E. Courtney, Reg. No. 36,491; Dennis J. Moore, Reg. No. 28,885; W. Daniel Swayze Jr., Reg. No. 34,478; Jay M. Cantor, Reg. No. 19,906		
SEND CORRESPONDENCE TO: Mark E. Courtney Texas Instruments Incorporated Mail Station 3999 P.O. Box 655474 Dallas, TX 75265		DIRECT TELEPHONE CALLS TO: Mark E. Courtney (972) 917-5632 (972) 917-4418 Fax
NAME OF INVENTOR: (1) **Sami Kiriaki**	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
3300 Caravan Drive **Plano, Texas 75025**	RESIDENCE & POST OFFICE ADDRESS:	RESIDENCE & POST OFFICE ADDRESS:
COUNTRY OF CITIZENSHIP: **U.S.A.**	COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: Sami Kiriaki	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 11/28/99	DATE:	DATE: